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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,683	07/24/2001	Austin H. Lesea	X-895 US	7141

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/912,683	LESEA, AUSTIN H.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-20* is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are presented for examination.

Drawings

The drawings were received on May 11, 2004. These drawings are acceptable. Therefore the objections to the drawings have been withdrawn.

Claim Rejections - 35 USC § 112

The 35 U.S.C. 112 second paragraph issues have been addressed and the rejections withdrawn in the response received on May 11, 2004.

Response to Arguments

Applicant's arguments filed May 11, 2004 with respect to claims 1-4, have been fully considered but they are not persuasive.

The purpose of a SERDES would necessarily be to transform data for further processing by other circuits and the fact that a programmable logic array can be programmed for a specific function and then reprogrammed for another function is the obvious in view of the purpose of BIST. Therefore the previous rejection of claims 1-4 is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Kean et al. U.S. Patent No. 5,737,235.

As per claims 1-4 Kean et al. teach allowing the same pad to be used for both configuration and user interface, making partial dynamic reconfiguration convenient, and offers the user choices for controlling logic functions from within the FPGA and choices for interfacing with structures outside the FPGA. It also allows the FPGA chip to be loaded with configuration information either from parallel address and data pins or from a serial data pin. In an FPGA integrated circuit chip, a programmable switch is placed between the pins or pads of the chip and the internal circuitry of the chip. The internal circuitry includes logic which is accessed by a user during operation of the FPGA and configuration memory which controls the functions performed by the FPGA chip. The programmable switch adopts an initial state upon power-up to connect selected external pins to the configuration memory so that the configuration memory can be loaded. However, the configuration memory programs not only the internal circuitry accessed by the user but also the programmable switch itself. Thus as configuration proceeds, or after configuration is completed, the programmable switch can be reconfigured to connect signal lines of the FPGA user logic to lines for addressing or controlling the configuration memory which were initially loaded from external pins. A programmable switch which is initially configured to connect its related pad or pads to configuration control lines can later be configured to connect an

internally generated signal or signals to the line or lines and thus override any external signal which would have been connected to that line or lines. (Column 4 line 40 through column 5 line 40, figure 17)

Claims 5-20 are allowable.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

The present invention pertains to a field programmable gate array (FPGA) device, which includes a high-speed serializer/deserializer (SERDES). The field programmable gate array allows programmable built-in testing of the SERDES at operating speeds. A digital clock manager circuit allows clock signals coupled to the SERDES to be modified during the test operations to stress the SERDES circuit. The logic array of the FPGA can be programmed to generate test patterns and to 'analyze data received by the SERDES Circuit. Cyclic redundancy check (CRC) characters, or other error checking characters, can also be generated using the logic array. During testing, the FPGA can perform extensive tests on the communication circuitry and store the results of the testing. An external tester can read the results of the test without substantial test time or complicated test equipment. After testing is complete, the device may be re-programmed to perform the end-user function, adding zero cost to the device for test implementation. The claimed invention (claim 5 as representative of the broadest independent claim) recites features such as "...input and output data communication connections; a serializer/deserializer circuit coupled to the input and

output data communication connections; and a logic array programmed to generate a test data pattern coupled to the output data communication connection, the logic array is further programmed to check a data pattern received on the input data communication connection while performing a built in self test operation." By coupling the SERDES to the user logic, the data may now be used for something other than configuration. This is a broader use of the SERDES, and may be used for telephony, data communications, data processing, and data switching applications. By utilizing existing user programmable logic to perform test functions, that same logic may be reprogrammed by the customer to then provide the intended application/use with no added cost.

The disadvantage of the prior arts is that the data can only be used for configuration, and the same logic cannot be reprogrammed *by the customer* to provide the intended application/use with no added cost. Therefore, the prior arts fail to teach "...input and output data communication connections; a serializer/deserializer circuit coupled to the input and output data communication connections; and a logic array programmed to generate a test data pattern coupled to the output data communication connection, the logic array is further programmed to check a data pattern received on the input data communication connection while performing a built in self test operation." As such, modification of the prior art of record can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time this invention was made, would have made the necessary modifications to the prior art of record to

encompass the limitations set forth in claims 5-20 of the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the claimed inventions. Hence, claims 5-20 are allowable over the prior arts of record.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cb

Cynthia Britt
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100